REMARKS

Claims 1-25 are pending in the present application.

Claim Rejections-35 U.S.C. 102

Claims 1-16 and 18-25 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Kobayashi et al. reference (U.S. Patent Application Publication No. 2002/0143517). This rejection is respectfully traversed for the following reasons.

The circuit for detecting an abnormal operation of memory of claim 1 includes in combination a delay circuit "for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto"; and a comparison circuit "for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted delay information operating part 12 and logical simulation part 10 in Fig. 1 of the Kobayashi et al. reference respectively as the delay circuit and the comparison circuit of claim 1. Applicant however respectfully submits that delay information operating part 12 of the Kobayashi et al. reference cannot be interpreted as the delay circuit of claim 1. Particularly, delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference does not delay output data from memory 14, and does not subsequently output the delayed output data responsive thereto, as

would be necessary to meet the features of claim 1.

As described in paragraph [0034] of the Kobayashi et al. reference with respect to Fig. 1, delay information operating part 12 is designed to receive the design net list F2, the dispersion rule file F4 and the library information "to prepare a delay information file F8", and to supply delay information file F8 to logical simulation part 10. As described in paragraph [0038] of the Kobayashi et al. reference, dispersion rule file F4 includes information for defining dispersion in a chip with electrical and physical characteristics which influence the operation of a semiconductor integrated circuit.

As further described beginning in paragraph [0043] of the Kobayashi et al. reference with respect to Fig. 2, the simulation system operates whereby library information from memory 14, the design net list F2 and dispersion rule file F4 are input to delay information operating part 12 shown in Fig. 1. Thereafter, delay information operating part 12:

> ***"executes a delay information operation for every cell which is described in the design net list F4 on the basis of the inputted information (step S4) and prepares a delay information file (which is generally an SDF file) F8 to supply the prepared file to the logical simulation part 10 (step S5)".***

Preparation of the delay information file F8 is described beginning in paragraph [0047] of the Kobayashi et al. reference, whereby the delay information operating part 12 calculates a corrected value of a propagation delay time of the two-input AND gates

shown in Figs. 4A and 4B. The description of the SDF files for both of the AND gates are respectively shown in paragraphs [0048] and [0049] of the Kobayashi et al. reference. That is, the information as output delay information operating part 12 as the delay information file F8 is shown in paragraphs [0048] and [0049].

As should be readily clear in view of the above noted description, delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference does not 1) receive data from memory 14, 2) delay the received data from memory 14, and 3) output the delayed data received from memory 14. In contrast, delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference receives library information from memory 14, design net list F2 and dispersion rule file F4, and executes a delay information operation for every cell which is described in design net list F4, and prepares a delay information file SDF F8 as shown in paragraphs [0048] and [0049] of the Kobayashi et al. reference. Accordingly, delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference cannot be interpreted as the delay circuit of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation memory of claim distinguishes over the Kobayashi et al. reference, and that this rejection of claims 1-7 is improper for at least these reasons.

With further regard to this rejection, as described in paragraph [0058] of the Kobayashi et al. reference, logical simulation part 10 incorporates a verifying test pattern and library information stored in memory 14, **executes a logical simulation**, and compares the result of the simulation with an expected value in the verifying test

pattern, to cause display part 16 to display the result of comparison. **That is, logical simulation part 10 in Fig. 1 of the Kobayashi et al. reference compares the result of simulation with an expected value in a verifying test pattern.** Logical simulation part 10 does not compare an output from memory 14 with a delayed output from memory 14, as would be necessary to meet the further features of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 distinguishes over the Kobayashi et al. reference as relied upon by the Examiner, and that this rejection of claims 1-7 is improper for at least these additional reasons.

Regarding claim 2, paragraphs [0059], [0097] and [0103] of the Kobayashi et al. reference do not describe or even remotely suggest detecting abnormal operation with regard to an access speed of memory. These particular paragraphs of the Kobayashi et al. reference as referred to by the Examiner do not specifically consider access speed of a memory. Applicant therefore respectfully submits that the circuit of claim 2 distinguishes over the Kobayashi et al. reference as relied upon by the Examiner for at least these additional reasons.

With further regard to this rejection, paragraph [0058] of the Kobayashi et al. reference does not describe a circuit that holds address information in the case of noncoincidence responsive to a noncoincidence signal, as would be necessary to meet the features of claim 3. As described in paragraph [0058] of the Kobayashi et al. reference, when **simulation** is not coincident with the expected value, design net list F2

is modified. Address information and/or a circuit for holding address information is not described or even remotely considered in paragraph [0058] of the Kobayashi et al. reference. Applicant therefore respectfully submits that the circuit of claim 3 distinguishes over the Kobayashi et al. reference as relied upon by the Examiner, and that this rejection of claim 3 is improper for at least these additional reasons.

With further regard to this rejection, paragraphs [0058] and [0083] and claim 6 of the Kobayashi et al. reference do not disclose that delay information operating part 12 in Fig. 1 delays an output of memory 14 to provide a delayed output, whereby the delay time is adjustable. That is, delay information file SDF F8 is not a delayed version of data output from memory 14 in Fig. 1 of the Kobayashi et al. reference. Applicant therefore respectfully submits that the circuit of claim 6 distinguishes over the Kobayashi et al. reference as relied upon by the Examiner, and that this rejection of claim 6 is improper for at least these additional reasons.

The integrated circuit of claim 8 includes in combination a memory; a delay circuit "which delays an output data from the memory and outputs a delayed data responsive thereto"; and a comparison circuit "which compares the output data from the memory and the delay data, and which outputs a noncoincidence signal when the output data and the delay data are not coincident".

As asserted above with respect to claim 1, delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference executes a delay information operation for every cell which is described in design net list F4 on the basis of inputted information and

prepares a delay information file F8. Delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference does not delay an output data from memory 14, and does not subsequently output the delayed data responsive thereto. Moreover, the logical simulation part 10 in Fig. 1 of the Kobayashi et al. reference executes a logical simulation, and subsequently compares the result of the simulation with an expected value in a verifying test pattern. Logical simulation part 10 in Fig. 1 of the Kobayashi et al. reference does not compare data from memory 14 with a delayed version of data from memory 14. The delay information operating part 12 and logical simulation part 10 in Fig. 1 of the Kobayashi et al. reference therefore cannot respectively be interpreted as the delay circuit and the comparison circuit of claim 8. Applicant therefore respectfully submits that the integrated circuit of claim 8 distinguishes over the prior art as relied upon by the Examiner, and that this rejection of claims 8 and 18 is improper for at least these reasons.

With further regard to this rejection, the Kobayashi et al. reference as relied upon does not store address information in an address information storing circuit when a comparison circuit outputs a noncoincidence signal, as would be necessary to meet the features of claim 18.

Applicant also respectfully submits that the method for detecting an abnormal operation of memory of claim 9 would not have been obvious in view of the relied upon prior art for at least somewhat similar reasons as set forth above with respect to claim 1. Particularly, delay information operating part 12 in Fig. 1 of the Kobayashi et al.

reference does not delay an output data output from memory 14, and does not subsequently output the delayed output data responsive thereto. Moreover, logical simulation part 10 in Fig. 1 of the Kobayashi et al. reference does not output a noncoincidence signal when output data from memory 14 and delayed data are not coincident with each other. Applicant therefore respectfully submits that the method for detecting an abnormal operation of memory of claim 9 distinguishes over the Kobayashi et al. reference as relied upon by the Examiner, and that this rejection of claims 9-16 is improper for at least these reasons.

With further regard to this rejection, Applicant respectfully submits that the Kobayashi et al. reference as specifically relied upon does not detect access speed of memory as featured in claim 10, and does not hold address information in case of noncoincidence in response to a noncoincidence signal as featured in claim 11. Moreover, since delay information operating part 12 in Fig. 1 of the Kobayashi et al. reference does not delay output data from memory 14, the Kobayashi et al. reference clearly does not disclose an adjustable delay time as featured in claim 15. Applicant therefore respectfully submits that claims 10, 11 and 15 would not have been obvious for at least these additional reasons.

Applicant also respectfully submits that the integrated circuit of claim 19 distinguishes over the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above. Accordingly, this rejection of claims 19-25 is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claim 17 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kobayashi et al. reference in view of the Fujiwara et al. reference (U.S. Patent No. 5,640,508). Applicant respectfully submits that the Fujiwara et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon Kobayashi et al. reference. Accordingly, Applicant respectfully submits that claim 17 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

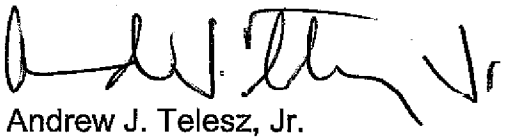
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to November 18, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $460.00 should be charged to Deposit Account No. 50-0238.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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